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UTILITY PATENT
APPLICATION TRANSMITTAL LETTER

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Sir:

Enclosed for filing is the utility patent application of Hoi-Sing KWOK, Fei-Hong YU, Qing-Cheng LI and Wing-Chiu YIP for METHOD AND APPARATUS FOR DRIVING REFLECTIVE BISTABLE CHOLESTERIC DISPLAYS.

Also enclosed are:

[X] 4 sheet(s) of [ ] formal [X] informal drawing(s);

[ ] a claim for foreign priority under 35 U.S.C. §§ 119 and/or 365 is [ ] hereby made to _ filed in __ on ___;
[ ] in the declaration;

[ ] a certified copy of the priority document;

[ ] a Constructive Petition for Extensions of Time;

[X] 1 statement(s) claiming small entity status will follow;

[X] an Assignment document will follow;

[ ] an Information Disclosure Statement; and

[X] Other: unexecuted Declaration.

The declaration of the inventor(s) [ ] also is enclosed [X] will follow.

[ ] Please amend the specification by inserting before the first line the sentence --This application claims priority under 35 U.S.C. §§119 and/or 365 to _ filed in _ on _; the entire content of which is hereby incorporated by reference.--

The filing fee has been calculated as follows [ ] and in accordance with the enclosed preliminary amendment:

CLAIMS					
	NO. OF CLAIMS		**EXTRA CLAIMS**	**RATE**	**FEE**
Basic Application Fee					$790.00
Total Claims	16	MINUS 20 =	0	x $22.00	-0-
Independent Claims	2	MINUS 3 =	0	x $82.00	-0-
If multiple dependent claims are presented, add $270.00					
Total Application Fee					790.00
If verified Statement claiming small entity status is enclosed, subtract 50% of Total Application Fee					395.00
Add Assignment Recording Fee of $40.00 if Assignment document is enclosed					
TOTAL APPLICATION FEE DUE					**$395.00**

[X] A check in the amount of $ 395.00 is enclosed for the fee due.

[ ] Charge $ _____ to Deposit Account No. 02-4800 for the fee due.

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Respectfully submitted,

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BACKGROUND

FIELD OF THE INVENTION

This invention relates to bistable cholesteric displays and, in particular, although not necessarily solely, a method and apparatus for driving reflective bistable cholesteric displays.

DESCRIPTION OF THE PRIOR ART

Bistable cholesteric liquid crystal displays "BCD" are already well known and utilized in a number of applications. The bistable cholesteric display usually consists of two pieces of glass forming a thin liquid crystal cell. The liquid crystal material is usually composed of twisted nematic liquid crystal heavily doped with a chiral dopant to give the liquid crystal a strong twist sense or chirality. Such cholesteric liquid crystal displays exhibit two stable states at a zero driving voltage. The first of these is the reflective planar "P" state and, as the name suggests, is reflective in normal usage. The second state is the scattering/transparent focal conic (FC) state. In normal usage, the FC state is transparent.

When used in conjunction with a dark light absorber placed at the back of the display, the FC state will appear black and the P state would appear to be bright when the display is viewed in reflection. The colour of the bright state can be adjusted by varying the chirality and pitch of the liquid crystal material. Such bistable liquid crystal displays are discussed in literature such as the monograph by S. Chandrasekhar entitled "Liquid Crystals" (Cambridge University Press, 1977).

A number of schemes have been developed to drive such bistable displays in a passive matrix manner. United States patent No. 4571585 by Stein et al. utilizes a wave form applied to the individual pixels which has been specially tailored in order to avoid cross talk problems. A number of voltage levels are needed for matrix driving of the display making

the invention rather cumbersome. An alternative matrix driving scheme is disclosed in the document entitled "A High Information Content Reflective Cholesteric Display" (SID 95 Digest, 1995) by Pfeiffer et al. In this scheme, commercial LCD driver chips were used and the display was scanned with 20 ms pulses. An upper voltage of 41 V would give the P state and a lower voltage of 33 V would produce the FC state. The scanning speed of 20 ms per line was achieved. However, this scheme has the disadvantage of a high voltage requirement and the relative slowness in scanning.

A more complicated dynamic driving scheme is discussed in the document entitled "Cholesteric Reflective Display: Drive Scheme and Contrast" (Appl. Phys. Lett., 64, 1905, 1994) by Yang et al. In this scheme, a 1 ms addressing time was shown to be possible although was only provided at the expense of more complicated wave forms and driver electronics. Again, the voltages required were quite high at greater than 40 V.

A further drawback in the dynamic scheme of Yang et al. is the appearance of a dark band in the display. A yet further disadvantage is that the image does not appear instantaneously. Instead, there is a 300 ms delay due to the slow switching from the FC state to the P state. A yet further disadvantage is that the contrast ratio of the dynamic driving scheme is very sensitive to the amplitude of the evolution voltage. The 1 ms addressing time shown to be possible at the expense of more complicated electronics is discussed in documents entitled "Dynamic Drive for Bistable Reflective Cholesteric Displays: A Rapid Addressing Scheme (SID 95 Digest, p.347, 1995) and "High Performance Dynamic Drive Scheme for Bistable Reflective Cholesteric Displays" (SID 96 Digest, p.359, 1996).

Faster switching to the P state has been demonstrated recently in a specially aligned BCD discussed in the document by M.H. Lu (Journal of Applied Physics, 81, 1063, 1997).

Even with this faster switching available with a specially aligned BCD, it still takes approximately 10 ms for the switching.

OBJECT OF THE INVENTION

It is an object of the present invention to provide a method and apparatus for the driving of a bistable cholesteric liquid crystal display that can utilize simpler electrical wave forms and is capable of faster line addressing speed to overcome some of the disadvantages of the prior art or at least provide the public with a useful choice.

SUMMARY OF THE INVENTION

The present invention provides a method of driving a bistable cholesteric liquid crystal display comprising setting the display initially to the P state. Once the liquid crystal display has completely switched to the P state, the entire panel is scanned line by line in the same manner as in conventional passive matrix super twisted nematic LCDs to switch the selected pixels from the P state to the FC state. The non-selected pixels are allowed to remain in the P state.

The present invention also provides a bistable cholesteric liquid crystal display driven in this manner. The driver provides an initial pulse or pulse train to set or reset the display to the P state. The display contains a matrix of overlapping electrodes such that one set of electrodes may be driven by an address pulse and the second set of electrodes in the display driven with data pulses. The pixels defined by the overlapping regions between the two sets of electrodes are switched by the selected pixels receiving an address pulse and data pulse which are cumulative while the non-selected pixels receive a voltage of the address pulse

minus the data pulse. Selection of the voltages are chosen such that the selected pixels will switch from the P state to the FC state and the non-selected pixels will remain in the P state.

In a final stage of the driving cycle, the display is allowed to stay without any driving voltages applied. This is the viewing phase of the driving scheme.

Further aspects of the invention may be considered novel when considered by those skill in the art to which the invention relates.

BRIEF DESCRIPTION OF THE DRAWINGS

The preferred embodiments of the invention will now be discussed with reference to the following drawings in which:

Fig. 1 shows a plot of the reflectance of a BCD cell against the voltage of the switching pulse;

Fig. 2 provides a plot of the switching voltage against time to show the switching of the BCD from the P state to the FC state;

Fig. 3 is a plot showing the switching history between the P and FC states in an example of the invention;

Fig. 4 shows an example of the timing sequence of a driving scheme in accordance with this invention;

Fig. 5 is a plot showing the influence of the non-selection pulse train on the P state pixel;

Fig. 6 is a cross sectional view through the basic structure of a liquid crystal display in accordance with one embodiment of the invention and,

Fig. 7 shows an electrode pattern for inclusion in a BCD cell in accordance with a preferred embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The invention will now be described with reference to preferred embodiments and experimental embodiments.

This invention seeks to provide a driving method and apparatus for bistable cholesteric liquid crystal displays. The invention is based on the observation that whereas switching from the FC state to the P state of the cholesteric liquid crystal display takes 0.3 s, switching from the P state to the FC state can take less than 1 ms.

A preferred embodiment of the driving scheme sets the whole LCD panel to the P state by the application of either a single pulse or a pulse train with a duration of T_r and an amplitude of V_r. This is referred to as the reset pulse. Typically, T_r can be 20 ms and V_r can be 40 V.

A time T_p is allowed for the liquid crystal display to complete the switch to the P state. The entire LCD panel may then be scanned line by line in the same manner as conventional passive matrix super twisted nematic LCDs. Such LCDs typically provide a matrix of electrodes which are generally provided as two sets of substantially orthogonal electrodes. These will be referred to as horizontal address lines or horizontal rows and vertical data lines or vertical columns in the subsequent description. Of course, the exact arrangement of the electrodes may be varied in accordance with alternative structures without departing from the general application of the invention. The terms "horizontal" and "vertical" are used for convenience to refer to the different substantially perpendicular sets of electrodes in the preferred embodiment. They are not intended as a restriction to the spacial arrangement or alignment of the electrodes or the display itself.

In the preferred embodiment, the horizontal address lines are driven by address pulses of amplitude V_s and a duration of T_s. The vertical data lines are driven with data pulses of

amplitude $\pm V_d$ and duration T_s. The pixels in the display are provided by the overlapping regions of the electrodes. The selected pixels for the display are subjected to a voltage of $V_s + V_d$ while the non-selected pixels will receive a voltage of $V_s - V_d$. Selection of the values of V_s and V_d may be chosen such that the selected pixels are switched from the P state to the FC state on receiving the total of the voltages and the non-selected pixels are allowed to remain below the threshold in the P state.

The display may then be allowed to stay without any driving voltages applied. This is the viewing phase of the driving scheme. The viewing duration can be of any length and the viewing time may be periodic or irregular in duration.

Thus, in the overall driving scheme to refresh the display in the BCD in the preferred embodiment, there are three stages. The display may be refreshed or reset, subsequently scanned and the final stage is the viewing of the display.

It is observed that addressing time of T_s of less than 1 ms per line is possible in a preferred embodiment. Such addressing time per line is already good enough for many applications such as the displays in pagers, cellular phones, personal data banks, etc. Even for a 100 line display panel, the total writing time is only 0.1 s at such an addressing speed. Furthermore, the scanning and data voltages may be kept quite low. In a preferred embodiment, the voltages V_s and V_d are 24 V and 6 V respectively. Such low voltages can be provided by commercial super twisted nematic liquid crystal display drivers.

In the preferred embodiments, the reset voltage V_r may be the maximum high voltage required. This may generally fall in the range of 40 V to 25 V depending on the reset pulse duration required. For a 40 V reset pulse, the reset pulse duration can be as small as 10 ms. For a 25 V reset pulse, the reset pulse duration has to be somewhat longer. Furthermore, as the reset pulse need not be applied all to one electrode, it can be shared between the row

and column or horizontal and vertical electrodes in order to reduce the voltage requirement. For applications which do not require frequent or fast resetting, the lower voltage may be preferred.

EXPERIMENTAL DATA AND EXAMPLES

To implement the method in a preferred embodiment, a low voltage cell has to be made. Several test cells were made. In a particular preferred embodiment, the cell gap of the sample LCD cell was 5 μm. The liquid crystal was provided with a homogeneous alignment and a mixture of a chiral dopant and ZLI 6204 were used in the sample cells. Although these are provided in the preferred embodiment, other nematic liquid crystals can also be used.

The response of the BCD cell to pulses of various voltages was measured using the following procedure. First the cell was driven to the reflective P state by a refresh pulse. The stabilized reflectance of the cell was measured as a function of the voltage of a switching pulse. This procedure was repeated with the cell in the FC state initially. Both the width of the applied switching pulse and the refresh pulse were 10 ms in this measurement. The pulse duration was changed in other measurements taken.

In this particular experiment, the central wave length of the incident light sources was 514 nm. The pitch of the BCD cell was adjusted to match that accordingly. As a result, the incident light is near perpendicular to the cell surface.

The results of this experiment are shown in Fig. 1. It can be seen that the curve P-FC-P represents the response of the cell originally in the P state prior to the application of the switching pulse. It can be observed that for voltages below 10 V, the reflection is not affected by the switching pulse. When the voltage of the pulse is between 10 V and 16 V,

the reflection decreases approximately linearly with increasing voltage. Therefore, a stable gray scale can be obtained in this region. It can be noted that the reflectance of the cell reaches its original value when the voltage is above 30 V.

The other curve, FC-P, shows the switching behaviour of the cell when it was in the FC state prior to the switching pulse. In this case, the reflectance of the cell is unchanged by the switching pulse of amplitudes below 22 V. The cell is switched to the P state by voltages above 28 V. For both the FC-P and P-FC-P curves, the reflectance contrast between the FC and P states is about 20:1. This value is among the better values for BCDs as reported in prior literature. The voltage values of $V_1 = 10$ V, $V_2 = 18$ V and $V_3 = 30$ V are lower than those reported in prior literature.

Referring now to Fig. 2, this figure shows the temporal behaviour of the switching from the P to the FC state. The upper curve is the applied voltage while the lower curve shows the measure reflectance. It can be observed from Fig. 2 that switching from the P state to the FC state occurs early on in the pulse and is complete in approximately 1 ms. Although the switching time is shown to be 1 ms, the switching pulse cannot be reduced to 1 ms itself as yet. It was found that if the switching pulse was reduced to 1 ms, the reflectance would rise back up again. Instead, a holding voltage is needed to stabilize the FC state. As shown in Fig. 2 for this preferred embodiment, the holding voltage is provided by the 10 ms switching pulse itself.

In the driving scheme of this preferred embodiment, reliance is provided on the column signal to hold the FC state after initial switching by a 1 ms pulse. In this example of a multiplex driving scheme, the pixel voltage consists of the difference between the scanning pulse train provided on the horizontal or row electrodes and the data pulse train provided on the vertical or column electrodes. As a result, the pixel voltage will have a

noise-like data pulse train together with the selection pulse. These data pulses can be used to hold the FC state after the initial switching.

The reflectance of a simulated selected pixel in this preferred embodiment is shown in Fig. 3. It can be seen that the pixel voltage consists of the initial 20 ms duration ±30 V refresh pulse which sets the pixel to the P state. This is followed with a 1 ms ±30 V switching pulse which is provided on top of a ±6 V background pulse train. This provides the switching and holding and it can be seen that the switching from the P to FC states is complete with appropriate contrast.

In Fig. 4, a new driving scheme is shown for a binary BCD. Although gray scale is possible from the observed linear nature of the reflection shown in Fig. 1, the preferred embodiment discussed herein provides a simpler binary BCD. It should be noted that such a gray scale driving scheme may be provided utilizing this invention.

The preferred driving scheme is shown in Fig. 4. According to the scheme, both the select and non-select pixels will see a 10-20 ms ±30 V pulse in the beginning. This is the reset pulse to refresh the display to a bright P state. Line by line scanning begins after a 0.1 s development time. In this multiplexing scheme, a select pixel will see the sum of the 1 ms address pulse (±24 V) and the data pulse (±6 V). As a result, the select pixels will see a ±6 V data train together with a 1 ms ±30 V selection pulse. This will cause the select pixels to switch to the FC state. In contrast, in the non-select pixel, the data pulse reverses sign. Therefore, the non-select pixels receive the same data train plus a 1 ms ±18 V pulse. It is important to make sure that, in the particular embodiment provided, the P state is not affected by this non-selection pulse. The voltages are chosen to allow the cumulative effect on selected pixels to exceed the threshold for switching to the FC state while the non-selected pixels do not exceed this threshold.

Referring to Fig. 5, this figure shows the influence of the data pulse train and the 1 ms $\pm$18 V pulse on the P state pixel for this preferred embodiment. It can be seen that the P state remains a P state. However, the reflectance has decreased by about 15%. This generally represents the cross talk between the select and non-select pixels. Further optimization may be desirable to reduce this cross talk.

There appears to be a direct correlation between the duration of the switching pulse, i.e. the addressing speed, and the amount of cross talk. For long switching pulses, the voltage required for switching from P to FC states can be reduced. Therefore the P state will be less affected by the cross talk.

In a further example, a 2 ms pulse for switching from P to FC states was used. It was observed that there was a significant reduction in cross talk in this embodiment. Therefore, the ultimate selection of the addressing speed can be compromised against the brightness and contrast of the display. It is also noted that in this preferred example, the P state appears substantially robust against small voltage perturbations occurring during the scanning with 0.5 ms pulses. However, the contrast and brightness are somewhat reduced.

Having scanned the display to select the pixels, this leaves the matters of the holding time and viewing time in this embodiment. Both are related to the last few lines of the panel.

Referring to Fig. 4, a 0.1 s $\pm$6 V pulse train is added to the end of the data pulse train. This is provided to stabilize the FC state for the last few lines of the panel where the 1 ms 30 V switching pulse appears at the end of the data pulse train. This holding pulse train can be reduced to 0.05 s in this preferred embodiment if necessary.

The viewing time is also needed for the last few lines of the panel. The last few lines of the panel are addressed last and pixel selection will appear at a time later than at the top

of the screen. For example, for a 100-line display, the time difference is some 0.1 s. Therefore, a longer viewing time may be desirable between frames in order to equalize the brightness between the first and last parts of the screen to be addressed. In most applications of BCDs, the display does not have to be refreshed frequently. This is particularly the case for pagers, cellular phone displays and other such examples. Therefore, the difference of 0.1 s or even 1 s for a 1,000-line display does not appear to be a significant disadvantage.

The apparatus of this preferred embodiment may include a bistable cholesteric liquid display as shown in Fig. 6. Fig. 6 sets out the basic structure of such a liquid crystal display. Generally such displays comprise two pieces of glass or similar transparent material 2 between which the cholesteric liquid crystal material 3 is provided.

On either side of the liquid crystal material, there is provided a patterned electrode layer 5.

In many instances, although not necessary, an alignment layer 4 is provided on one or both sides of the crystal material.

When incorporated into a full display, a light absorbing black layer may be provided on the back of the liquid crystal display such as layer 6 in Fig. 6. Although a variety of light absorbing layers may be used, typically such layers comprise a layer of black cloth or velvet or even black paint or similar.

Referring to Fig. 7, the electrode pattern for a preferred embodiment is shown. The electrode pattern may provide a matrix of electrodes wherein the electrode layers on both sides of the liquid crystal material form a regular pattern of electrodes. As shown in this example in Fig. 7, an upper layer of electrodes 5A are provided as a series of substantially parallel electrodes and the lower layer 5B are again substantially parallel and substantially

perpendicular to the upper level. The matrix itself provides a series of overlapping regions which may form the pixels of the display.

Although shown as substantially perpendicular rows and columns, the electrode pattern could be changed to form alternative pixel patterns and displays as desired.

Referring again to Fig. 6, each of the electrode layers receives electrical pulses from a suitable pulse generator 7 and 8. The pulse generators may be provided by a series of electrical or electronic components. An associated input control or processing means 9 may provide the desired signal to the electrical pulse generators 7 and 8 to display any particular message.

In general, the voltages provided to each of the row and column electrodes are periodic with each period corresponding to one frame of the display. Furthermore, the voltages within one frame period as provided by the drivers are divided into separate phases being the reset phase, data scanning phase and viewing phase.

In such liquid crystal displays, the electrodes 5A and 5B are provided by a transparent conductive film. Again, a number of materials may be utilized although indium tin oxide is common to form the pixilated display.

The optional alignment layer 4 is regularly provided by a coating of polymer on the transparent conductive films such that the polymer may provide alignment to the cholesteric liquid crystal.

The liquid crystal display cell gap can be chosen to suit the particular application. In this preferred embodiment, a cell gap range of 4 to 20 μm is sufficient.

It should also be noted that the drivers for the electrodes 7 and 8 may provide voltages in each frame period which invert in sign relative to an adjacent frame. The pulses provided may include a reset pulse duration of between 1 to 100 ms in this preferred example

and the reset phase duration in this example may be 20 ms to 0.3 s. There is no requirement that the reset pulse duration and reset phase duration be the same.

The drivers 7 and 8 may provide reset voltages between 10 to 40 V in this embodiment. This need not be applied to a single electrode layer but instead may be the result of a reset pulse split between the electrodes. In any particular example, the reset pulse can be provided entirely on the row electrodes 5B or the column electrodes 5A with zero V on the other electrode respectively. Alternatively, it may be a result of a combination of voltages on the electrodes.

The address pulse and data pulse provided by the drivers 7 and 8 in this preferred example may be in the range of 0.5 to 10 ms in duration. This will provide a display wherein the data scanning phase may be 0.5 to 10 ms times the number of row electrodes in duration.

The preferred output of the address pulse voltage is approximately 24 $\pm$3 V and the data pulse voltage is preferably approximately 6 $\pm$2 V.

It may also be preferable that the row and column voltages may be biased by the same constant voltage within each frame. This can result in the same pixel voltage.

The viewing phase provided in the display may be longer than 0.1 s in duration for the preferred embodiment.

Although the time period consisting of the reset phase, data scanning phase and viewing phase can be referred to as periodic, this may not be a regular period. Instead, this may vary as required. As such, the liquid crystal display may be driven only on demand.

Thus it can be seen that this invention provides a method and apparatus for driving bistable cholesteric liquid crystal displays which, at least in a preferred form, is capable of 1 ms per line addressing speed. The actual addressing speed may be compromised to reduce

cross talk or other matters according to the particular application. It can utilize simple electrical wave forms and relies on the faster switching from the P to FC states to provide the faster addressing speed. Although the display requires a reset to the P state, the invention may still be particularly useful for types of data displays where refreshing is not as frequent.

Specific items mentioned in this disclosure are deemed to incorporate equivalents known to those skill in the art to which the invention relates. This scope of the invention is not intended to be restricted by the described preferred embodiments but instead defined by the appended claims.

CLAIMS

1. A method of driving a bistable cholesteric liquid crystal display comprising the steps of:

- providing a reset voltage to set the pixels in the display to the reflective P state;
- switching selected pixels to provide the desired pattern to the FC state and;
- holding said display for a suitable viewing period.

2. A method of driving a bistable cholesteric liquid crystal display as claimed in claim 1 wherein said method comprises providing electrical pulses to column and row electrodes to impart a voltage on the cholesteric liquid crystal material in each pixel to drive the switching between the P state and the FC state.

3. A method of driving a bistable cholesteric liquid crystal display as claimed in claim 2 wherein said reset voltage is in the range of 10 to 40 V.

4. A method of driving a bistable cholesteric liquid crystal display as claimed in claim 2 wherein said step of providing electrical pulses to electrodes to switch said selected pixels to the FC state to provide said display comprises driving one set of electrodes with an address pulse and the remaining set of electrodes with data pulses such that the selected pixels are subjected to a voltage being the sum of the address and data pulses which is greater than the threshold voltage to switch to the FC state and the

non-selected pixels received a voltage with a data pulse of inverse sign to be a voltage below the threshold for switching to the FC state.

5. A method of driving a bistable cholesteric liquid crystal display as claimed in claim 2 wherein said viewing phase comprises applying insufficient voltages to any pixels to cause a change from the P state to the FC state.

6. A bistable cholesteric liquid crystal display comprising:

- a bistable cholesteric liquid crystal display;
- a plurality of pixels within said display;
- driving means to apply voltage to each pixel; and
- control means controlling said driving means to supply an initial voltage to said pixels to set all pixels to the P state, subsequently supplying sufficient voltage to selected pixels to switch said pixels to the FC state to provide the desired pattern and maintaining said display for a period of time for viewing of the display.

7. A bistable cholesteric liquid crystal display as claimed in claim 6 wherein said display includes a matrix of overlapping electrodes with the pixels of the display being defined by overlapping regions of said matrix of electrodes.

8. A bistable cholesteric liquid crystal display as claimed in claim 7 wherein said matrix of overlapping electrodes comprises a first set of electrodes and a second set of electrodes with the pixels defined by the overlapping regions between said first and

second sets of electrodes and wherein the reset voltage from the driving means is provided to said electrodes to drive all said pixels to the P state.

9. A bistable cholesteric liquid crystal display as claimed in claim 8 wherein the voltage supplied to the pixels for the display comprises providing an address voltage to one set of electrodes and a data voltage to the remaining set of electrodes such that selected pixels receive a cumulative total of said voltages and non-selected pixels receive a data voltage of opposite sign to provide a lower total voltage to non-selected pixels.

10. A bistable cholesteric liquid crystal display as claimed in claim 9 wherein said address pulse voltage is approximately 24 $\pm$3 V.

11. A bistable cholesteric liquid crystal display as claimed in claim 9 wherein said data pulse voltage is approximately 6 $\pm$2 V .

12. A bistable cholesteric liquid crystal display as claimed in claim 6 wherein said electrodes comprise transparent conductive film.

13. A bistable cholesteric liquid crystal display as claimed in claim 11 wherein said transparent conductive film comprises indium tin oxide.

14. A bistable cholesteric liquid crystal display as claimed in claim 6 wherein said liquid crystal cell has a gap of 4 to 20 μm.

15. A bistable cholesteric liquid crystal display as claimed in claim 6 wherein the liquid crystal display is driven only on receipt of a signal by the control means.

16. A bistable cholesteric liquid crystal display as claimed in claim 6 wherein said display is incorporated in a pager or cellular telephone.

ABSTRACT

This invention provides a method and apparatus for driving bistable cholesteric liquid crystal displays. The method and apparatus provided a display in which all the pixels are initially driven to the P state. Selected pixels for the display are then driven to the FC state to provide the desired message. The state of the pixels is then maintained for a viewing period prior to any resetting of the display to the P state. The switching from the P state to the FC state allows faster addressing times and lower voltages to be used in driving the display.

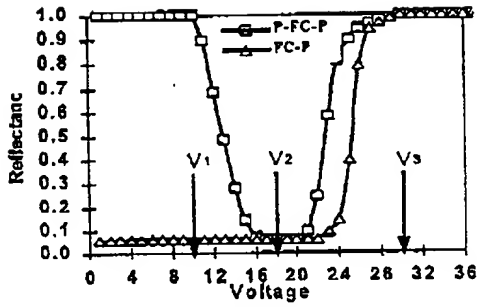

Fig. 1 Reflection of the BCD cell vs the voltage of switching pulse.

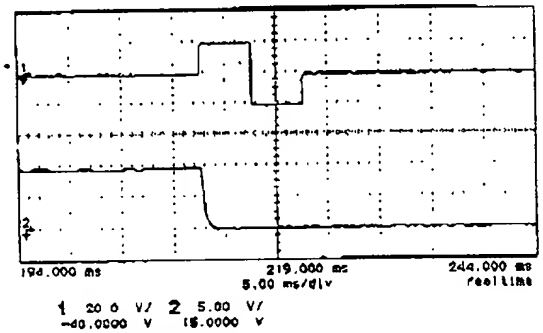

Fig. 2 The switching of the BCD from the P state to FC state. The response time is about 1 ms.

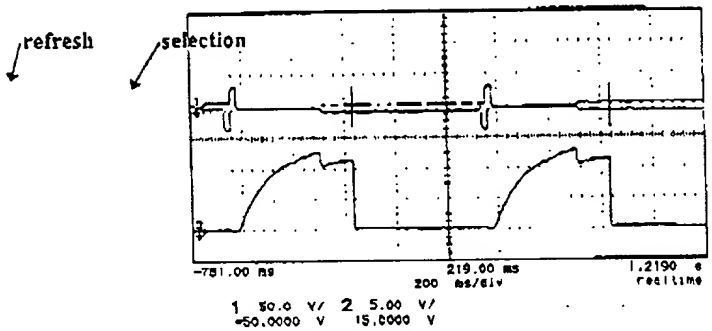

Fig. 3 Switching history between the P and FC states.

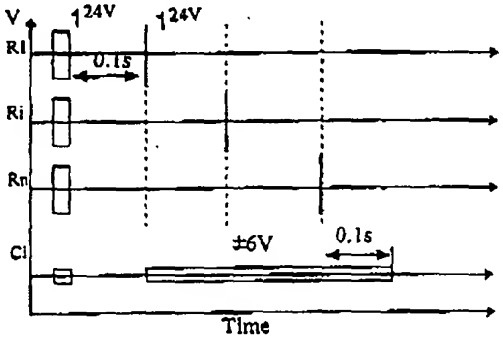

Fig. 4 Timing sequence of the driving scheme. Ri is the row signal and Ci is the column signal.

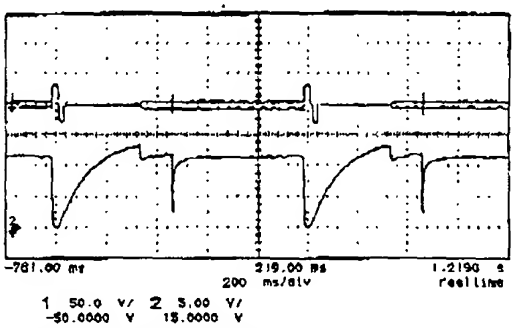

Fig. 5 Influence of the nonselection pulse train on the P state pixel.

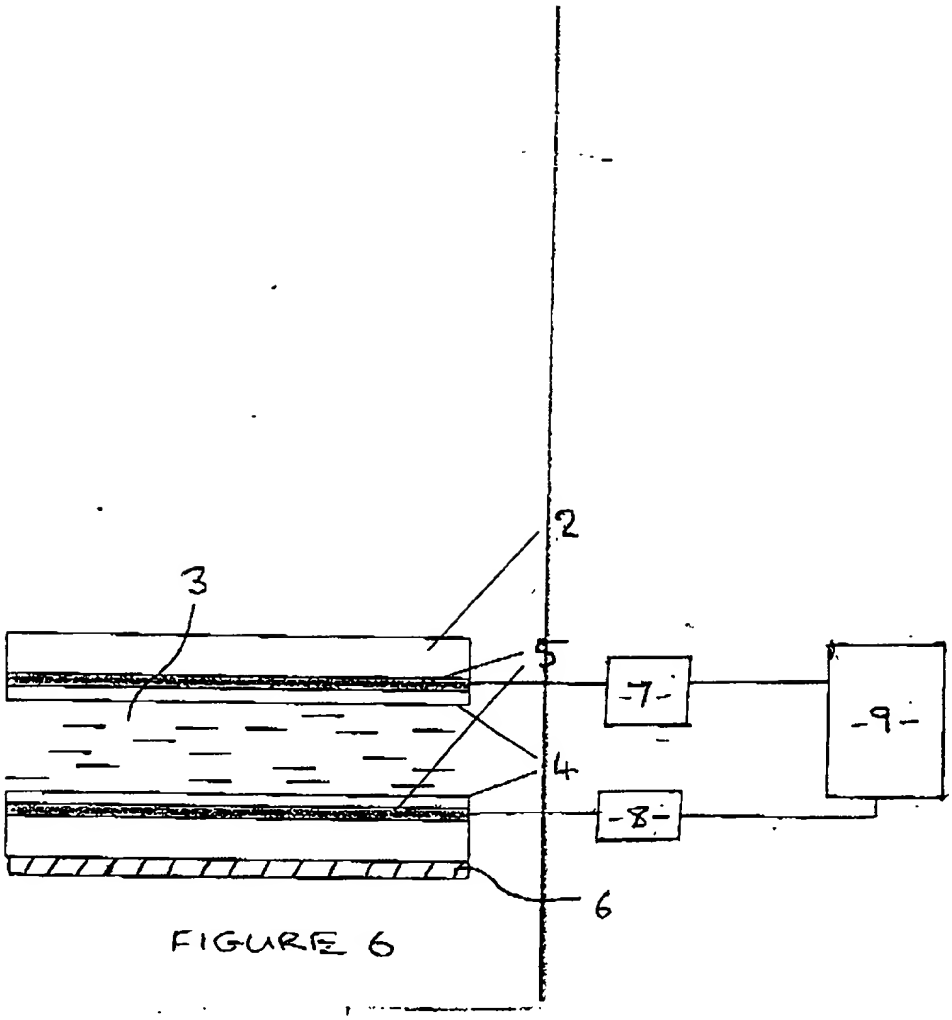

FIGURE 6

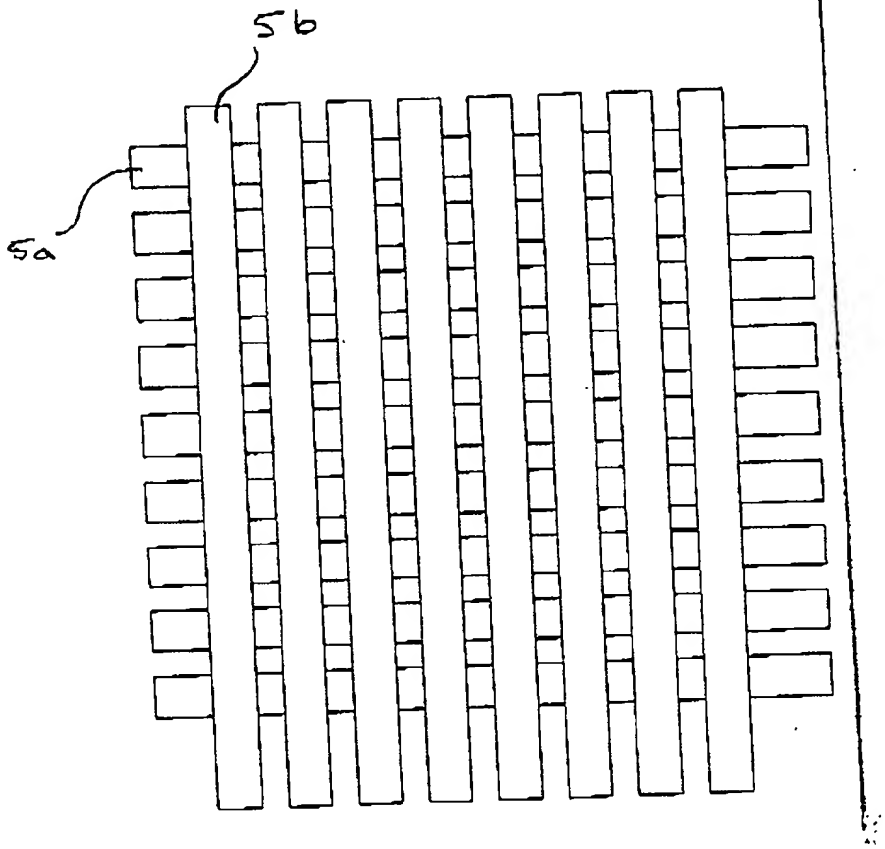

FIGURE 7

COMBINED DECLARATION AND POWER OF ATTORNEY FOR UTILITY PATENT APPLICATION	Attorney's Docket No. 007198-334

As a below-named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name;
I BELIEVE I AM THE ORIGINAL, FIRST AND SOLE INVENTOR (if only one name is listed below) OR AN ORIGINAL, FIRST AND JOINT INVENTOR (if more than one name is listed below) OF THE SUBJECT MATTER WHICH IS CLAIMED AND FOR WHICH A PATENT IS SOUGHT ON THE INVENTION ENTITLED:

METHOD AND APPARATUS FOR DRIVING REFLECTIVE BISTABLE CHOLESTERIC DISPLAYS

the specification of which

(check one) ☒ is attached hereto;

☐ was filed on _____ as

Application No. _____

and was amended on _____ (if applicable);

I HAVE REVIEWED AND UNDERSTAND THE CONTENTS OF THE ABOVE-IDENTIFIED SPECIFICATION, INCLUDING THE CLAIMS, AS AMENDED BY ANY AMENDMENT REFERRED TO ABOVE;

I ACKNOWLEDGE THE DUTY TO DISCLOSE TO THE OFFICE ALL INFORMATION KNOWN TO ME TO BE MATERIAL TO PATENTABILITY AS DEFINED IN TITLE 37, CODE OF FEDERAL REGULATIONS, Sec. 1.56 (as amended effective March 16, 1992);

I do not know and do not believe the said invention was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to said application; that said invention was not in public use or on sale in the United States of America more than one year prior to said application; that said invention has not been patented or made the subject of an inventor's certificate issued before the date of said application in any country foreign to the United States of America on any application filed by me or my legal representatives or assigns more than twelve months prior to said application;

I hereby claim foreign priority benefits under Title 35, United States Code Sec. 119 and/or Sec. 365 of any foreign application(s) for patent or inventor's certificate as indicated below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application(s) on which priority is claimed:

COMBINED DECLARATION AND POWER OF ATTORNEY		Attorney's Docket No. 007198-334	
COUNTRY/INTERNATIONAL	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
			YES_ NO_
			YES_ NO_

I hereby appoint the following attorneys and agent(s) to prosecute said application and to transact all business in the Patent and Trademark Office connected therewith and to file, prosecute and to transact all business in connection with international applications directed to said invention:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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